Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (currently amended): A program verify circuit for nonvolatile memory cells, comprising:

a) a nonvolatile memory chip,

b) a bit line read path,

c) a reference read path,

d) a voltage control circuit connected in said bit line read path and said reference read path,

e) a sense amplifier,

f) an equalizer circuit to make voltages stored on the bit line read path and the reference read path a same amplitude, and

g) an output node of the bit line read path and the output node of the reference read path connected to said sense amplifier inputs.

Claim 2. (currently amended) The circuit of claim 1, wherein the voltage control circuit further comprises:

a) a band gap reference generator,

b) a digital to analog converter,

c) an NMOS switching device, and

d) said band gap generator controls the digital to analog converter (DAC) to produce a set of voltages at an output of the DAC to control said voltage control circuit.

Claim 3. (previously presented) The circuit of claim 2, wherein the output of said DAC is coupled to all said control circuits in said memory chip to insure said set of voltages are applied to all said control circuits.

Claim 4. (currently amended) The circuit of claim 1, wherein the bit line read path further comprises:

a) a selected nonvolatile memory cell from within a plurality of memory cells coupled to a bit line of the bit line read path,

b) a column decoder circuit, and

c) a load device.

Claim 5. (previously presented) The circuit of claim 4, wherein the load device couples a chip voltage to the bit line read path and charges the output node of the bit line read path when the control circuit isolates the selected bit line from the bit line read path.

Claim 6. (currently amended) The circuit of claim 1, wherein the reference read path further comprises:

a) a dummy memory cell coupled to the reference read path, and

b) a reference line decoder.

Claim 7. (previously presented) The circuit of claim 6, wherein said dummy memory cell provides a reference line load similar to that of a memory cell on a bit line read path.

Claim 8. (previously presented) The circuit of claim 1, wherein the voltage control circuit in the bit line read path charges the bit line to a precharge voltage and then decouples the bit line from the output node of the bit line read path.

Claim 9. (previously presented) The circuit of claim 1, wherein the control circuit in the reference read path charges the reference read path to a precharge voltage.

Claim 10. (currently amended): A method of verifying the programming of a nonvolatile memory cell, comprising:

a) selecting a bit line read path coupled to a nonvolatile memory cell that is being verified for a program operation,

b) connecting an output node of a bit line read path and an output node of a reference line read path to a sense amplifier,

c) charging a bit line coupled to the bit line read path to precharge voltage,

d) charging a reference line of the reference line read path to said precharge voltage,

e) equalizing the bit line voltage and the reference line voltage, and then floating said reference line at the precharge voltage level,

f) disconnecting said bit line from said output node of said bit line read path, charging said output of the bit line read path to a high chip voltage that is larger than the precharge voltage,

g) selecting said memory cell allowing said bit line to be discharged, and if said bit line voltage drops to below a predetermined voltage level, then coupling said bit line voltage to said output node of the bit line read path and discharging the output node of the bit line read path to a voltage below said precharge voltage, and

h) comparing output voltages of the bit line read path and the reference line read path using said sense amplifier to determine if the selected cell is programmed.

Claim 11. (previously presented): The method of claim 10, wherein said sense amplifier compares the output voltage of the bit line read path to the output voltage of the reference line read path after a predetermined period of time.

Claim 12. (previously presented): The method of claim 10, wherein charging said output of the bit line read path to a high chip voltage is done through a load device coupled to an external memory chip bias V_{DD}.

Claim 13. (previously presented): The method of claim 10, wherein equalizing the bit line voltage and the reference line voltage insures a same value exists on both the bit line and the reference line.

Claim 14. (currently amended): The verification of a program operation to a nonvolatile memory cell, comprising:

a) a means for charging a selected bit line connected to a nonvolatile memory cell to a predetermined voltage and isolating said bit line from a bit line output node while maintaining the predetermined voltage charge,

b) a means for charging a reference line to a predetermined voltage and isolating said reference line while maintaining the predetermined voltage charge,

c) a means for equalizing the voltage charge between the selected bit line and the reference line,

d) a means for charging said bit line output node to a voltage larger than said predetermined voltage while maintaining isolation from said selected bit line,

e) a means for discharging said output node to a voltage below said predetermined voltage when said nonvolatile memory cell is in an erase state, and

f) a means for comparing voltages on said output node and said reference line to determine if said memory cell has been programmed.

Claim 15. (previously presented): The verification of the program operation of claim 14, wherein the means for charging and isolating said selected bit line is performed by a bit line read path control circuit.

Claim 16. (previously presented): The verification of the program operation of claim 14, wherein the means for charging and isolating said reference line is performed by a reference line control circuit.

Claim 17. (previously presented): The verification of the program operation of claim 14, wherein the means for charging said bit line output node to said voltage larger than the predetermined voltage is through a load transistor connected to a high voltage chip bias.

Claim 18. (previously presented): The verification of the program operation of claim 14, wherein the means for discharging the output node uses the selected memory cell, which is in an erase state, to discharge the output node.

Claim19. (previously presented): The verification of the program operation of claim 14, wherein the means for comparing voltages uses a sense amplifier coupled to the output node and the reference line.

Claim 20. (currently amended): A program verify circuit, comprising:

a) a nonvolatile memory cell connected in a bit line read path containing a bit line column decoder circuit, a voltage control circuit, an output node and a load device connected to memory chip bias,

b) said output node coupled to said input of the sense amplifier,

c) said voltage control circuit coupled to a clamping transistor that in turn couples a verify reference voltage to an input of a sense amplifier,

d) said voltage control isolates said bit line from said output node when said memory cell is programmed and allows the load device to charge the output node to a bias voltage,

e) said sense amplifier compares said verify reference voltage to said bias voltage if said memory cell is programmed, and

f) said sense amplifier compares said verify reference voltage to an erased cell voltage if said memory cell is erased.

Claim 21. (previously presented): The circuit of claim 20, wherein said voltage control circuit couples a read reference voltage to said clamping transistor and the input of the sense amplifier when performing a normal memory cell read operation whereby an output node voltage is compared to the read reference voltage.

Claim 22. (previously presented): The circuit of claim 20, wherein the comparison performed by the sense amplifier occurs after a predetermined amount of time.

Claim 23. (previously presented): The circuit of claim 20, wherein the bias voltage is larger than the verify reference voltage.

Claim 24. (previously presented): The circuit of claim 20, wherein the erased cell voltage is smaller than the verify reference voltage.

Claim 25. (currently amended): A method of verifying a program of a nonvolatile memory cell, comprising:

a) discharging a bit line coupled to a selected nonvolatile memory cell to ground,

b) charging said bit line,

c) isolating said bit line from an output node of a bit line read path when said memory cell is programmed thereby allowing said output node to charge further to an external chip bias,

d) coupling a verify reference voltage and an output voltage of said output node to sense amplifier inputs, and

d) comparing said verify reference voltage and said output voltage to determine if said memory cell is programmed.

Claim 26. (previously presented): The method of claim 25, wherein said output voltage is an erase voltage of the memory cell and is smaller than said verify reference voltage when the memory cell is not programmed.

Claim 27. (previously presented): The method of claim 25, wherein said output voltage is said external chip bias and is larger than said verify reference voltage when the memory cell is programmed.

Claim 28. (previously presented): The method of claim25, wherein said verify reference voltage is replace with a read reference voltage during a read operation of said memory cell.

Claim 29. (currently amended): A program verify operation for a nonvolatile memory cell, comprising:

a) a means for charging a bit line coupled to a nonvolatile memory cell,

b) a means for creating a verify reference voltage and coupling said verify reference voltage to a sense amplifier input,

c) a means for isolating said bit line from an output node of a bit line read path thereby allowing said output node to further charge to a chip bias voltage when memory cell is programmed, and

d) a means for comparing said verify reference voltage to a voltage on said output node after a predetermined amount of time.

Claim 30. (previously presented): The program verify operation of claim 29, wherein said means for comparing said verify reference voltage to said output node voltage compares the verify reference voltage to an erase voltage when said memory cell is erased.

Claim 31. (previously presented): The program verify operation of claim 30, wherein said means for comparing said verify reference voltage to said output node

voltage compares the verify reference voltage to an erase voltage where said erase voltage is smaller than said verify reference voltage.

Claim 32. (previously presented): The program verify operation of claim 29, wherein said means for comparing said verify reference voltage to said output node voltage compares the verify reference voltage to said chip bias where said chip bias voltage is larger than said verify reference voltage.